Course Syllabus

California State University, Bakersfield (CSUB)
Department of Electrical & Computer Engineering & Computer Science
ECE 3220: Digital Design with VHDL

Instructor
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Office: Room 322, Science Building III
Office hours: Tuesday, 13:00AM – 15:00PM

Lecture and Lab Sections
Lecture: Tu/Th, 11:30AM - 12:45PM, Science III, Room 313
Laboratory: Fri 10:00AM - 12:30PM, Science III, Room 313

Prerequisite:
ENGR/ECE/PHYS 2070 and ECE 3200

Recommended Textbooks

Supplementary books:
1. Digital systems design using VHDL, Charles H. Roth, JR
2. Digital Electronics a Practical Approach with VHDL, 9th edition, William Kleitz

Course Description:
The primary objective of this course is to teach students how to design digital systems using hardware description languages (HDL). The course provides design methodologies which partition a system into a data-path and controller and focuses on synthesizable RTL VHDL code for digital circuit design using dataflow, structural, and behavioral coding styles. The course introduces VHDL simulation and verification, and FPGA synthesis, placement, routing, timing analysis and performance optimization. The material covered in the lecture is reinforced through practical experience in the associated lab, including an emphasis on the use of VHDL to synthesize logic circuits.

Course Objectives:
In this course students will learn to:
• Design Basic Logic Circuits
• Design and Evaluate Combinational-Circuit Building Blocks
• Design and Test Circuits Employing Flip-Flops, Registers, Counters, and a Simple Processor
• Design and Analyze Synchronous Sequential Circuits
Topics to be covered in this course:
1. Digital Logic Review
2. Programmable Logic Device (PLD)
3. Basics of VHDL
4. HDL Modeling of Combinational Logics (Data flow, Structural and Behavioral Modeling)
6. Finite State Machines
7. RTL Design Methodology, Transition from Pseudocode & Interface to a Corresponding Block Diagram.
8. Central Processing Unit Design

Homework
Homework will be assigned on a weekly basis, covering the material discussed in class. It is due at the beginning of class on the date specified. Problems in each homework will be graded on the following basis: a correct answer gets 100%, a reasonable attempt gets 50%, and no attempt or a very poor attempt gets 0%. The assignments will be graded and returned within one week.
Late policy: No late submissions will be accepted, as solutions will be posted on the day after it is due.

Laboratory
The laboratory of this course consists of a set of experiments to complement the material covered in the lecture course. The majority of the laboratory experiments focus on the use of VHDL (hardware description language) by Quartus II (CAD tool) to design, simulate, synthesize, implement and test combinational and sequential logic circuits.

The experiments to be performed include:
- Lab 1. Quartus II Introduction Using Schematic Design
- Lab 2. Design of a BCD to 7-segment decoder using VHDL.
- Lab 3. BCD to 7 Segment LED Display Decoder Circuit
- Lab 4. Combinational Circuit Design
- Lab 5. Latches, Flip-Flops, and Registers
- Lab 6. Finite State Machines (FSM)

Attendance in lab is mandatory. The Lab reports will be graded and returned within one week.

Grading
Your final grade will be the weighted average of the homework, Lab, midterm and final exams, as calculate from the formula below:

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<tr>
<td>Assignments</td>
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<td>Labs</td>
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<td>Midterm exam</td>
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<td>Final exam</td>
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All students enrolled in this course must attend Final Exam. An absence at final exam will result in an ‘F’ grade in the course. If you have any conflict with the final exam date, you must notify me two weeks prior to the final exam.
Accessibility:
California State University, Bakersfield attempts to guarantee access to all classes by all students. Students can find CSUB's accessibility policies and services by going to the website for the Office of Services for Students with Disabilities. In addition, E-Learning Services at CSUB has its own policy for guaranteeing access to students in online classes:

"California State University, Bakersfield is committed to providing equal access to Web-based information for people with disabilities. This is in accordance with Section 504 of the 1973 Rehabilitation Act, Section 508 of the Rehabilitation Act Amendment of 1998 and the 1990 Americans with Disabilities Act, and Executive Order 926 of California State University."

To achieve the goal of universal accessibility, CSUB uses Blackboard as its Learning Management System (LMS), the first LMS to receive the Nonvisual Accessibility Gold Certification by The National Federation of the Blind. Students can read more about Blackboard's guarantee of accessibility and its accessibility programs at its website.

Technical Requirements and Support:
All of the lectures in this class were given in PDF. Adobe Acrobat Reader is available on every computer on the CSUB campus. If students have difficulty with the content of the class, they need to contact the instructor. If students are having any technical problems with Blackboard, or loading the IPA fonts from Blackboard to their own computers, then students need to contact the Blackboard Help Desk, either by telephone (661) 654-2315 or by email lmssupport@csub.edu. Students may also go to the E-Learning Services Building on the east side of the Walter Stiern Library.